

Graduate School of
Information, Production and Systems,
Waseda University

Field [System LSI]

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Title [Professor]

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Yasuaki Inoue was born in Niigata (a region with heavy snowfalls), Japan, in 1945. He received the D.E. degree in electronics and communication engineering from Waseda University. From 1964 to 2000, he was with Sanyo Electric Co., Ltd., Gunma, Japan, where he was engaged in research and development in analog integrated circuits and analog/digital EDA systems. He holds over forty patents. The figure (lower right) is the EDA system developed by him. In Sanyo Semiconductor Company, he was General Manager of the EDA Technology Department and the Memory Development Department. From 2000 to 2003, he was a Professor with University of East Asia, Shimonoseki, Japan. Since 2003, he has been a Professor with the System LSI Field, the Graduate School of Information, Production and Systems, Waseda University, Kitakyushu, Japan. It is his motto to have no likes and dislikes in human beings (as well as wines).



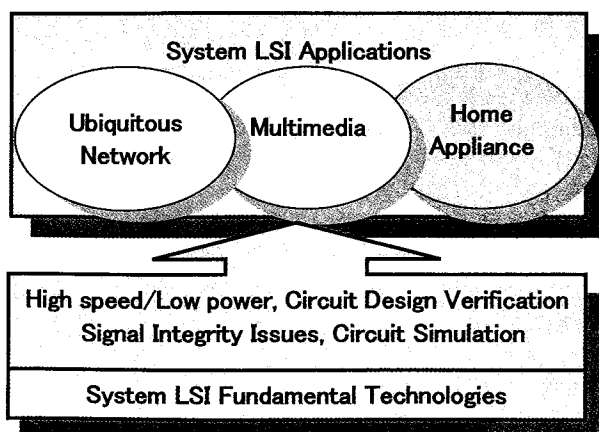
No likes and dislikes
in human beings
(as well as wines).

RESEARCH INTERESTS: His research interests include analog circuits, EDA systems, and numerical analysis of nonlinear circuits and systems. Among those, as fundamental technologies toward next generation system LSI applications for ubiquitous network, multimedia, and home appliance, currently he has been focusing his research interests on high-speed circuit design technologies, low power circuit design technologies, circuit design verification technologies, signal integrity issues, and advanced circuit simulation technologies as shown in the figure (lower left). He succeeded in solving record-breaking large-scale analog circuits (nonlinear circuit equations with 40,000 variables) by his unique algorithm based on the homotopy continuation method. The record has not been broken yet. The analog is one of most important keywords for next generation system LSI fundamental technologies, by which the Kitakyushu Science and Research Park has been aiming at the central position in the region of Asian system LSI industries.

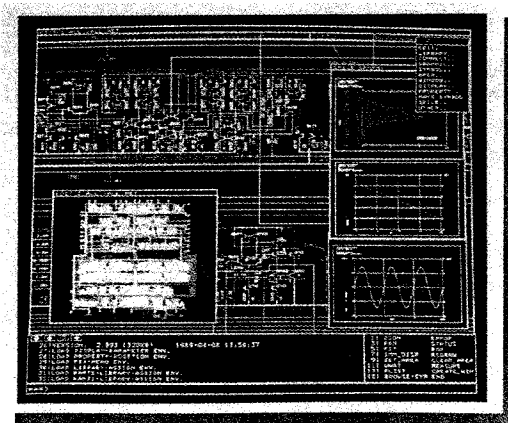
PROFESSIONAL ASSOCIATIONS: He is a member of IEICE, IPSJ, IEEJ, and IEEE. From 1997 to 1999, he was an Associate Editor of the IEEE Transactions on Circuits and Systems Part II.

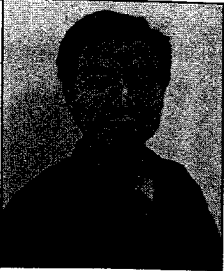
AWARDS: He received the Ishikawa Award from the Union of Japanese Scientists and Engineers in 1998, the Engineer Award from the Gunma Prefecture in 1999, the Distinguished Service Award from the Science and Technology Agency, the Japanese Government in 1999, the TELECOM System Technology Award from the Telecommunications Advancement Foundations in 2002, the Achievement Award from the Information Processing Society Japan in 2003, and the Funai Information Technology Promotion Award from the Funai Foundation for Information Technology in 2004.

Research area



EDA System developed by him



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学位(授与機関)	PhD, Tsinghua University (Dept. of Computer and Science), Peking, China		取得年	2005
(1) 主要な研究テーマ又は研究領域等				
研究テーマ・研究領域	Optimization techniques and their applications to Electronic Design Automation, especially, floorplanning, placement, high-level synthesis, Design For Manufacturability, etc.			
キーワード	Electronic Design Automation, Floorplanning, Placement, High-level Synthesis, Design For Manufacturability			
当該テーマ・領域の概要及び特徴	<p>The EDA (Electronic Design Automation) is a large interdisciplinary research field. It is also called Computer-Aided Design (CAD) of Integrated Circuits. As the advance of silicon technology, the EDA researchers are faced many new challenges, e.g., process variability, reliability, power, etc.</p> <p>The knowledge of circuits (circuit design, microelectronics, circuit manufacturing), algorithms (graph algorithms, complexity theory), mathematics, and computer-aided design are necessary. Many problems from EDA field are complicated multi-objective and multi-constraint optimization problem. The proper formulations and the efficient and effective problem-specific heuristics have to be found to solve these problems.</p>			
主な論文・著書又は研究活動	<p>[1] Song Chen, Liangwei Ge, Mei-Fang Chiang, Takeshi Yoshimura, "Lagrangian Relaxation Based Inter-Layer Signal Via Assignment for 3-D ICs", IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, Vol.E92-A, No.4, pp. 1080-1087, April, 2009.</p> <p>[2] S. Chen and Takeshi Yoshimura, "Fixed-outline Floorplanning: Enumerating Block Positions and A New Objective Function for Calculating Area Costs", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol.27, No.5, 2008, pp. 858-871.</p> <p>[3] S. Chen, S. Dong, X. Hong, and C. Cheng, "Vlsi block placement with alignment constraints," IEEE Transactions on Circuits and Systems II: Express Briefs, , vol. 53, no. 8, pp. 622-626, 2006.</p> <p>[4] S. Chen, X. Hong, S. Dong, and et al, "Fast evaluation of bounded slice-line grid," Springer Journal of Computer Science and Technology, vol. 19, no. 6, pp. 973-980, 2004.</p> <p>[5] S. Chen, X. HONG, S. Dong, and et al, "A buffer planning algorithm for chip-level floorplanning," Science in China Series F-Information Sciences, vol. 47, no. 6, pp. 763-776, 2004.</p> <p>[6] Y. Ma, X. Hong, S. Dong, S. Chen, and et al, "Buffer planning as an integral part of floorplanning with consideration of routing congestion," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 24, no. 4, pp. 609-621, 2005.</p> <p>[7] L. Ge, S. Chen, K. Wakabayashi, T. Takenaka, T. Yoshimura, "Max-flow Scheduling in High-level Synthesis", IEICE Trans. on Fundamentals of Electronics, Communications and Computer Sciences, vol. E90-A, no. 9, pp. 1940-1948, 2007.</p>			
応用可能な分野	Design automation of System LSI, especially physical design tools.			
(2) 企業向けメッセージ				
(3) 学外活動・学会活動				
IEEE Member, IEICE Member.				
(4) その他				