## **Zhejiang University Information & Electronic Engineering Students Summer Program**Week 1

Sunday	Monday	Tuesday	Wednesday	Thursday	Friday	Saturday
Day 1	Day 2	Day 3	Day 4	Day 5	Day 6	Day 7
Arrive in Los Angeles  Grocery Shopping  Dinner  Apartment Check-in	9:00am - 10:00am Welcome Ceremony Program Orientation  10:00am - 12:00pm Campus Tour  12:00pm - 1:30pm Welcome Luncheon  1:30pm - 4:30pm Lecture: Innovation and entrepreneurship situation  ENTREPRENEURS	9:00am - 12:00pm Lecture: Review Digital Signal Processing Concepts, Time domain response of FIR and IIR filters  1:30pm - 1:30pm Lunch Break  1:30pm - 4:30pm Lecture Design and Implementation of Filters with FPGA Board Basys 3 (6 Hands-on Labs using Simulink/Xilinx for Analysis and Simulation)	9:00am – 12:00pm Visit: University of California, Los Angeles  Visit: University of Southern California	9:00am - 12:00pm Lecture: Frequency Domain Response of FIR and IIR filters, Comb filters, Notch filters, Digital Sinusoidal Oscillators (1)  12:00pm - 1:30pm Lunch Break  1:30pm - 4:30pm Lecture: Design and Implementation of Filters with FPGA Board Basys 3 (6 Hands-on Labs using Simulink/Xilinx for Analysis and Simulation)	9:00am - 12:00pm Lecture: Frequency Domain Response of FIR and IIR filters, Comb filters, Notch filters, Digital Sinusoidal Oscillators (2)  12:00pm - 1:30pm Lunch Break  1:30pm - 4:30pm Lecture: Design and Implementation of Filters with FPGA Board Basys 3 (6 Hands-on Labs using Simulink/Xilinx for Analysis and Simulation)	Universal Studio

## **Zhejiang University Information & Electronic Engineering Students Summer Program**Week 2

Sunday	Monday	Tuesday	Wednesday	Thursday	Friday	Saturday
Day 8	Day 9	Day 10	Day 11	Day 12	Day 13	Day 14
San Diego	8:30am – 12:00pm Lecture: American Science and Technology Development  1:2:00pm – 1:30pm Lunch Break  1:30pm – 4:30pm Lecture: Design and Implementation of Filters with FPGA Board Basys 3 (6 Hands-on Labs using Simulink/Xilinx for Analysis and Simulation)	9:00am - 12:00pm  Lecture: Design FIR and IIR filters (Floating/Fixed points)  for (val points)  1:00pm - 1:30pm Lunch Break  1:30pm - 4:30pm Lecture: Design and Implementation of Filters with FPGA Board Basys 3 (6 Hands-on Labs using Simulink/Xilinx for Analysis and Simulation)	9:00am – 12:00pm Visit: Hollywood Walk of Fame  12:00pm – 1:30pm Lunch Break  1:30pm – 4:00pm Visit: TCL Chinese Theater	9:00am - 12:00pm Lecture: Discrete Fourier Transform (DFT), Fast Fourier Transform (FFT) Discrete Fourier Series (1)  12:00pm - 1:30pm Lunch Break  1:30pm - 4:30pm Lecture: Design and Implementation of Filters with FPGA Board Basys 3 (6 Hands-on Labs using Simulink/Xilinx for Analysis and Simulation)	9:00am - 12:00pm Lecture: Discrete Fourier Transform (DFT), Fast Fourier Transform (FFT) Discrete Fourier Series (2)  12:00pm - 1:30pm Lunch Break  1:30pm - 4:30pm Lecture: Design and Implementation of Filters with FPGA Board Basys 3 (6 Hands-on Labs using Simulink/Xilinx for Analysis and Simulation)	Disney Land

## **Zhejiang University Information & Electronic Engineering Students Summer Program**

Week 3

Sunday	Monday	Tuesday	Wednesday	Thursday	Friday	Saturday
Day 15	Day 16	Day 17	Day 18	Day 19	Day 20	Day 21
Outlet SHOPPING!!	9:00am – 9:15am Lecture: Public Speaking Skills- Medical Conference Presentation Skills  12:00pm – 1:30pm Lunch Break  1:30pm – 4:30pm Lecture: Design and Implementation of Filters with FPGA Board Basys 3 (6 Hands-on Labs using Simulink/Xilinx for Analysis and Simulation)	9:00am - 12:00pm Lecture: Decimation and Interpolation  12:00pm - 1:30pm Lunch Break  1:30pm - 4:30pm Lecture: Design and Implementation of Filters with FPGA Board Basys 3 (6 Hands-on Labs using Simulink/Xilinx for Analysis and Simulation)	9:00am – 12:00pm Visit: East Village Arts District  12:30Pm – 3:30 pm  Visit: The Pike at Rainbow Harbor	9:00am - 12:00pm Lecture: Frequency Resolution for Target Detection  12:00pm - 1:30pm Lunch Break  1:30pm - 4:30pm Lecture: Design and Implementation of Filters with FPGA Board Basys 3 (6 Hands-on Labs using Simulink/Xilinx for Analysis and Simulation)	9:00am – 12:00pm Lecture: Design and Implementation of Filters with FPGA Board Basys 3 (6 Hands-on Labs using Simulink/Xilinx for Analysis and Simulation)  12:00pm-1:30pm Lunch Break  1:30pm – 4:30pm Students Final Demonstration and Presentation Graduation Ceremony	Apartment Checkout  Leave from LAX  Return to China

## **Zhejiang University Information & Electronic Engineering Students Summer Program**

We reserve the right to make changes to this schedule. Contact information:

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